CLAIMS

What is claimed is:

1. A method for manufacturing a DRAM cell including two active word lines having a common drain/source region and having distinct source/drain regions contacting two memory points, comprising, after the forming of insulated conductive lines on a semiconductor substrate, the steps of:

a) depositing a first insulating layer;

b) depositing a second insulating layer, selectively etchable with respect to the first insulating layer;

c) etching the second insulating layer to only maintain it above the insulated conductive lines, at least above an active region of the substrate;

d) depositing and leveling a third thick insulating layer selectively etchable with respect to the second insulating layer;

e) forming an opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench;

f) depositing a conductive material to fill the previously-formed opening;

g) performing a chem-mech polishing of the entire structure; and

h) depositing a fourth insulating layer, selectively etchable with respect to the third insulating layer.

2. The method of claim 1, wherein step e) consisting of forming the opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench is implemented to open the first and third insulating layers to at least also partially expose the source/drain regions, and wherein the conductive material deposited at step f) is deposited to fill all the openings thus formed.

3. The method of claim 1, wherein step e) consisting of opening the first and third insulating layers to at least partially expose the common drain/source regions and an insulating trench is preceded by the steps of:

i) opening the first and third insulating layers to at least partially expose the source/drain regions;

j) depositing a conductive material in the openings thus formed; and

k) performing a chem-mech polishing of the entire structure, whereby contacts are formed with the source/drain regions.

4. The method of claim 3, wherein step k) of chem-mech polishing is followed by the deposition of an additional insulating layer on the entire structure, step e) then consisting of successively opening the additional insulating layer and the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench.

5. The method of claim 1, wherein step g) of chem-mech polishing of the entire structure, or step h) of deposition of the fourth insulating layer, selectively etchable with respect to the third insulating layer, is followed by the steps of:

l) forming openings in said first and third insulating layers to at least partially expose the source/drain regions;

m) depositing a conductive material in the openings thus formed; and

n) performing a chem-mech polishing of the entire structure, whereby contacts are formed with the source/drain regions.

6. The method of claim 1, wherein step a) of deposition of the first insulating layer is preceded by the deposition of an additional insulating layer selectively etchable with respect to a filling material of underlying insulating trenches and with respect to the first insulating layer.

7. The method of claim 6, wherein the first and third insulating layers are made of silicon oxide and wherein the second and fourth insulating layers as well as the additional insulating layer are made of silicon nitride.

8. The method of claim 1, wherein the memory cell is formed in a same substrate as logic circuits.

9. A DRAM cell structure comprising:

two inactive word lines formed on insulating trenches, on either side of an active region of a substrate, and two active word lines having a common drain/source region and having distinct source/drain regions contacting two memory points, wherein the four word lines, the insulating trenches, and the substrate are covered at least partially with a multiple-layer of at least three insulating layers, formed of first and third layers deposited over the entire structure, and of a second layer removed from the active region, except above the word lines, and being made of a material selectively etchable with respect to the first and third layers, and wherein a bit line of the cell directly rests upon at least a portion of its drain/source region as well as on a neighboring insulating trench, the bit line and the third insulating layer being covered with a fourth insulating layer selectively etchable with respect to the third layer.

10. The structure of claim 9, wherein the multiple-layer rests upon an additional insulating layer selectively etchable with respect to the first superposed insulating layer and with respect to the filling material of the underlying insulating trenches.

11. A memory device, comprising:

a semiconductor substrate having an active region delineated by insulating trenches;

a plurality of word lines on the substrate, including first and second word lines;

a common drain/source region positioned in the active region between the first and second word lines;

a source and a drain region positioned respectively in the active region on opposite sides of the first and second word line with respect to the common drain/source region;

a plurality of insulating layers deposited over the plurality of word lines, including a first layer, removed from the active region except above the word lines, and second and third layers deposited over the entire active region and selectively etchable with respect to the first layer, the third layer being thicker than the first or second layers and leveled on an upper surface;

an opening in the second and third layers above the common drain/source region and a portion of the insulating trenches;

a conductive material filling the opening and forming a bit line of the memory device; and

a top insulating layer, selectively etchable with respect to the third insulating layer, deposited above the third layer and the conductive material.

12. The memory device of claim 11, wherein the first insulating layer lies between the second and third insulating layers.

13. The memory device of claim 12, wherein the plurality of insulating layers includes a fourth insulating layer, selectively etchable with respect to the second insulating layer and a filling material of the insulating trench, deposited between the semiconductor substrate and the second insulating layer.

14. The memory device of claim 11, further comprising:

additional openings in the second and third layers above the source and drain regions; and

a conductive material filling the additional openings.

15. The memory device of claim 11, wherein the top insulating layer is leveled on an upper surface.

16. The memory device of claim 11, wherein the conductive material is tungsten.

17. The memory device of claim 11, wherein the plurality of word lines further comprises third and fourth word lines on the semiconductor substrate and outside of the active region.